

Claims

What is claimed:

1. A memory back-up system comprising:
 - a first memory cell;
 - a non-volatile memory cell that is interfaced to the first memory cell;
 - control circuitry that allows data to be written to one of the first memory cell and the non-volatile memory cell, and that provides transfer of the data from one of the first memory cell and the non-volatile memory cell to the other one of the first memory cell and the non-volatile memory cell.
2. The memory back-up system of claim 1, wherein the control circuitry further includes allowing data to be read from one of the first memory cell and the non-volatile memory cell.
3. The memory back-up system of claim 1, wherein the first memory cell and the non-volatile memory cell are integrated on a common substrate.
4. The memory back-up system of claim 1, wherein the non-volatile memory cell is an MRAM memory cell.
5. The memory back-up system of claim 1, wherein the non-volatile memory cell comprises at least one of MRAM memory, ferro-electric FeRAM, and Flash memory.

6. The memory back-up system of claim 1, wherein the first memory cell is formed adjacent to a substrate, and the non-volatile memory cell is formed adjacent to the first memory cell.
7. The memory back-up system of claim 1, further comprising a plurality of first memory cells and a plurality of non-volatile memory cells.
8. The memory back-up system of claim 7, wherein the plurality of first memory cells and the plurality of non-volatile memory cells are integrated on a common substrate.
9. The memory back-up system of claim 7, wherein the plurality of first memory cells and the plurality of non-volatile memory cells are accessed through a common set of access control lines.
10. The memory back-up system of claim 9, wherein the common set of access control lines comprise at least one of row select lines and column select lines.
11. The memory back-up system of claim 7, wherein the plurality of first memory cells and the plurality of non-volatile memory cells comprise a shared set of wide data lines.
12. The memory back-up system of claim 11, wherein the shared set of wide data lines comprises at least 256 data lines.

13. A memory back-up system comprising:
- a volatile memory cell;
 - a non-volatile memory cell that is interfaced with the volatile memory cell;
 - a common control line connected to the volatile memory cell and the non-volatile memory cell, the common control line allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell.
14. The memory back-up system of claim 13, wherein the volatile memory cell is a DRAM memory cell and the non-volatile memory cell is an MRAM memory cell.
15. The memory back-up system of claim 13, further comprising a second control line which in combination with the common control line provides selection of the volatile memory cell.
16. The memory back-up system of claim 13, further comprising a third control line which in combination with the common control line provides selection of the non-volatile memory cell.
17. The memory back-up system of claim 13, further comprising a
- an array volatile memory cells;
 - an array of non-volatile memory cells, each non-volatile memory cell interfaced with a corresponding volatile memory cell;
 - a plurality of common control lines, each common control line connected to a corresponding plurality of volatile memory cells and the non-volatile memory cells, the common

control line allowing data to be simultaneously written to the corresponding plurality of volatile memory cells and the non-volatile memory cells.

18. A memory back-up system comprising:

- a plurality of first memory cells;

- a plurality of non-volatile memory cells that are interfaced to the first memory cells;

- control circuitry that allows data to be written to one of the first memory cells and the non-volatile memory cells, and that provides transfer of the data from one of the first memory cells and the non-volatile memory cells to the other one of the first memory cells and the non-volatile memory cells.

19. The memory back-up system of claim 18, wherein the control circuitry further includes

- allowing data to be read from one of the first memory cell and the non-volatile memory cell.

20. A computing device comprising:

- a controller;

- a memory unit interfaced with the controller, the memory unit comprising;

 - an array volatile memory cells;

 - an array of non-volatile memory cells, each non-volatile memory cell interfaced with a corresponding volatile memory cell; and

 - a plurality of common control lines, each common control line connected to a corresponding plurality of volatile memory cells and the non-volatile memory cells, the

common control line allowing data to be simultaneously written to the corresponding plurality of volatile memory cells and the non-volatile memory cells.

21. An image storing device comprising:

means for receiving an image;

a memory unit for storing the image, the memory unit comprising;

an array volatile memory cells;

an array of non-volatile memory cells, each non-volatile memory cell interfaced with a corresponding volatile memory cell; and

a plurality of common control lines, each common control line connected to a corresponding plurality of volatile memory cells and the non-volatile memory cells, the common control line allowing data to be simultaneously written to the corresponding plurality of volatile memory cells and the non-volatile memory cells.